EXPRESS MAIL NO. EV336655493US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Robert Louis Hodges
Filed	:	April 19, 2004
For	:	SELF-ALIGNED GATE AND METHOD

Docket No.	:	98-P-104D1 (850063.542D1)
Date	:	April 19, 2004

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents:

In accordance with 37 C.F.R. §§ 1.56 and 1.97 through 1.98, applicant wishes to make known to the Patent and Trademark Office the eight (8) references set forth on the attached form PTO-1449. This application relies, under 35 U.S.C. § 120, on the earlier filing date of prior Application No. 09/733,243, filed December 7, 2000. The references listed on the attached Form PTO-1449 were submitted to and/or cited by the Patent and Trademark Office in this prior application and, therefore, are not required to be provided in this application. If the Examiner wishes, copies will be provided upon request. As to any reference supplied, applicant does not admit that it is "prior art" under 35 U.S.C. §§ 102 or 103, and specifically reserves the right to traverse or antedate any such reference, as by a showing under 37 C.F.R. § 1.131 or other method. Although the aforesaid references are made known to the Patent and Trademark Office in compliance with applicant's duty to disclose all information he is aware of which is believed relevant to the examination of the above-identified application, applicant believes that his invention is patentable.

Please acknowledge receipt of this Information Disclosure Statement and kindly make the cited references of record in the above-identified application.

Respectfully submitted,

Seed Intellectual Property Law Group PLLC

Robert Iannucci
Registration No. 33,514

Enclosure:
Form PTO-1449

701 Fifth Avenue, Suite 6300
Seattle, Washington 98104-7092
Phone: (206) 622-4900
Fax: (206) 682-6031

303640_1.DOC

FORM PTO-1449 (REV.7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 98-P-104D1 (850063.542D1)	APPLICATION NO.
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		APPLICANT Robert Louis Hodges	
		FILING DATE April 19, 2004	GROUP ART UNIT

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA	4,378,627	04/05/83	Jambotkar	29	571	
	AB	4,419,810	12/13/83	Riseman	29	571	
	AC	4,758,528	07/19/88	Goth et al.	437	15	
	AD	5,027,185	06/25/01	Liauh	357	59	
	AE	5,434,093	07/18/95	Chau et al.	437	41	
	AF	5,597,752	01/28/97	Niwa	437	44	
	AG	5,637,516	06/10/97	Müller	438	203	
	AH	5,688,700	11/18/97	Kao et al.	437	29	
	AI	5,796,157	08/18/98	Fallico et al.	257	557	
	AJ						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES	TRANSLATION NO
	AK					
	AL					
	AM					
	AN					
	AO					

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	AP		IBM Technical Disclosure Bulletin, Vol. 28 #7 pp. 2767-2768, 12/85, 257/346
	AQ		IBM Technical Disclosure Bulletin, Vol. 31 #7 pp. 311-312, 12/88, 257/346
	AR		Wolf et al., "Silicon Processing for the VLSI", Volume 1, Pages 191-194, 1986.

EXAMINER	DATE CONSIDERED

* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).